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Design of FFT Algorithm in OFDM Communication System

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ABSTRACT
The present communication system is limited by three major factors. Those are System capacity, higher data rates and interference. To meet these requirements, 802.11-based wireless LANs has fascinated interest in providing higher data rates and greater system capacities. Among them, the 802.11a standard based on OFDM (Orthogonal Frequency Division Multiplexing) modulation scheme is defined to meet high-speed and large-system-capacity challenges. To implement OFDM System, FFT (Fast Fourier Transform) and IFFT (Inverse Fast Fourier Transform) are the major hardware requirements. The System capacity is increased by increasing the FFT processor size. Higher data rates are achieved by proper architecture of FFT.
This paper presents the design of a 256 point modified $Radix\ 2^2$ pipelined FFT/IFFT processor to achieve the higher data rates. And data constellation, symbol detection at transmitter and receiver is done by using QPSK (Quadrature Phase Shift Keying) Modulation for easy of designing in OFDM communication system. The design has been coded in Verilog and the simulations and synthesis are carried out by using Xilinx 9.2i.
KEYWORDS: OFDM, Radix 2^2 Algorithm, FFT, QPSK

I. INTRODUCTION

The OFDM modulation is realized by the Inverse Fast Fourier Transform (IFFT) that enables the use of a large number of subcarriers— up to 1024 according to the Mobile WiMAX system profiles to be accommodated within each OFDMA symbol. Before transmission, each OFDMA symbol is extended by its cyclic prefix at the transmitter. At the receiver end, cyclic prefix is discarded and OFDM demodulation is applied through the Fast Fourier Transform (FFT).

The Fast Fourier Transform (FFT) is most efficient algorithm to compute the Discrete Fourier Transform (DFT) and performs most important operations in modern digital signal processing and communication systems. Classical implementation of the FFT/IFFT architecture, with digital signal processors (DSPs), requires a sequential algorithm. This increases the execution time. On the other side, the present programmable circuits, like an FPGA, uses a tens of thousands of lists and triggers during process, resulting of parallel processing system, puts the FPGA computing speed at a significant advantage over DSPs.

This paper presents the implementation of a 256 point modified $\boldsymbol{Radix\ 2^2}$ pipelined FFT/IFFT processor. And also focuses on the QPSK for data constellation in OFDM.

II. ARCHITECTURE AND DESIGN METHODOLOGY

A. Modified $Radix\ 2^2$ Decimation in Frequency FFT Algorithm

The$Radix\ 2^2$ algorithm is used to clearly reflect the structural relation with radix-2 algorithm and the identical computational requirement with radix-4 algorithm.

The DFT of a sequence *x(n), n=0, 1,…, N-1* is defined as: *X(k), k=0, 1, …,N-1*

$$X(K) = \sum_{n=0}^{N-1} x(n)\, W_N{}^{nk} \quad \text{, for } 0 \le K < N \qquad (1)$$

Where $W_N = e^{-j2\pi/N}$ denotes the primitive *Nth* root of unity. The input sequence x(n) and its DFT is X(k).A 3-dimensional linear index map is applied by.

$$n =< D + n_3 >$$
$$K =< K_1 + 2C >$$

This yield

$$X(K_1 + 2C) = \sum_{n_3=0}^{\frac{N}{4}-1} \sum_{n_2=0}^{1} \sum_{n_1=0}^{1} x(D + n_3).W_N{}^{(D+n_3)(K_1+2C)}$$

(2)

Where, D = $\frac{N}{2}(n_1 + \frac{n_2}{2})$ and C = $2(K_2 + 2K_3)$

$X\ (K_1 + 2C)$

$$= \sum_{n_3=0}^{\frac{N}{4}-1} \left[M(K_1, K_2, n_3) {W_N}^P\right] W_{\frac{N}{4}}^{n_3 K_3} \quad (3)$$

Where, $P = n_3(K_1 + 2K_2)$

Where, $M(K_1, K_2, n_3)$ is expressed in eqn.

$$M(K_1, K_2, \mathrm{A}) = \left[x\left(\mathrm{A} - \frac{N}{2}\right) + (-1)^{K_1}\,\mathrm{x(A)}\right] + (-\mathrm{j})^{\overline{(\mathrm{A}-\frac{N}{2})}^{\mathrm{P}}} \left[\mathrm{x(A)} + (-1)^{K_1}\ \mathrm{x}\left(\mathrm{A} + \frac{N}{4}\right)\right] \quad (4)$$

After this simplification, a set of four DFTs of length *N/4* is obtained. Each term in equation (4) represents a Radix-2 butterfly (BFI), and the entire equation (4) also represents Radix-2 butterfly (BFII) with trivial multiplication by *–j*. Where, A=$n_3 + \frac{N}{2}$.

The *N*-point FFT processor has $\log_4(N)$-stages with *i* is the stage number. A typical stage consists of BFI, BFII, delay-feedback, ROM, and TFM. A $\log_2(N)$ counter is used to control the processor. The formation of the last stage is different according to the size of FFT; if *N* is power of 2, the last stage is formed by BFI only. But if *N* is power of 4, the last stage formed by BFI and BFII.

B. BFI structure

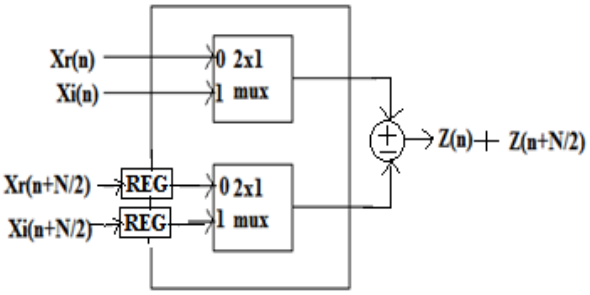

Fig: 1. BFI for $R2^2$ *pipeline FFT*

The detailed structure of BFI is shown in Fig.1. The first N/2 elements are applied to the first multiplexer and next N/2 elements are applied to the second multiplexer through pipeline registers. When both the multiplexer are switches to position '0' both the real parts are add/subtracted and stored in a shift register. When both the multiplexers are switches to position '1' both the imaginary parts add/subtracted and performs addition operation with data stored in the shift register.

C. BFII structure

The detailed structure of BFII is shown in Fig.2.The multiplication by *–j* involves real-imaginary swapping and inversion of sign. The multiplexors are used to swapping the real-imaginary terms and the sign inversion is handled by switching the adding-subtracting operations by mean of multiplexing. When there is a need for multiplication by *–j*, all multiplexors switches to position "1", the real-imaginary data are swapped and the adding-subtracting operations are switched.

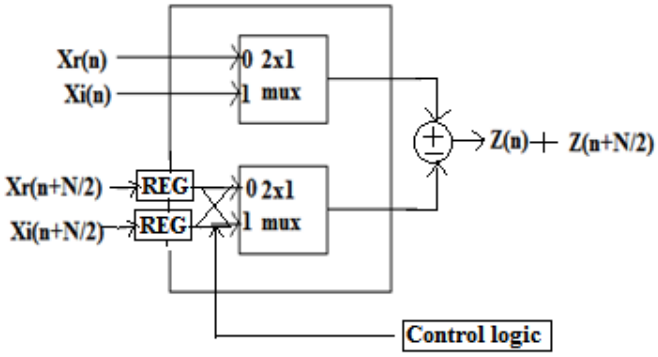

Fig: 2. BFII for $R2^2$ *pipeline FFT*

D TFM Structure

A six clock cycle fully-pipelined complex-multiplier has been implemented to multiply the twiddle factor by the output of BFII. According to Equation (5), the algorithm of multiplying the twiddle factor (a + *jb*) by BFII output (X*r* + *jXi*) uses four multipliers, one adder, and one subtractor.

$$(X_r + jX_i).(a + jb) = (X_r.a - X_i.b) + j(X_i.a + X_r.b)\ . \quad (5)$$

Twiddle factor generator is a key component in IFFT/FFT computation. There are many popular generation methods for twiddle factor generation. The twiddle factors are generated according to equation (6), converted to fixed point, and then stored in ROM. The twiddle factors at the i^{th} stage, with $i = 0,1,\ldots..,(\log_4 N) - 2$ is given by $W_i = \{u_x\}; x = 0,1,\ldots..,{}^{N}/_{2^{2i}}$ with $u_x = e^{-j2\pi m/N}$

$$m = \begin{cases} 0, & 0 \le x < p \\ 2^{2i+1}.(\mathrm{x} - \mathrm{p}), & p \le x < 2p \\ 2^{2i}.(\mathrm{x} - 2\mathrm{p}), & 2p \le x < 3p \\ 3.2^{2i}(\mathrm{x} - 3\mathrm{p}), & 3p \le x < 4p \end{cases} \quad (6)$$

$$\text{With,} \quad p = \frac{N}{2^{2i+1}}$$

E Delay-Feedback Structure

In Radix 2^2 signal flow graph at stage 0 the first N/2 elements has to be delayed until the next half of the elements presented, after that the calculations can proceed. If this delay is maintained at each stage it increases the processing time as the word length increases. In order to reduce these delays here pipeline registers are used at every stage preceding to the calculations. Due to this calculations are done simultaneously at all stages.

III. MODIFIED RADIX 2^2 FFT ARCHITECTURE

An implementation of the modified $R2^2$ pipeline architecture is shown in Fig.3. It uses two types of butterflies, one is same as that in R2SDF, the other contains the logic to implement the trivial twiddle factor multiplication, as shown in Fig.1 & 2 respectively.

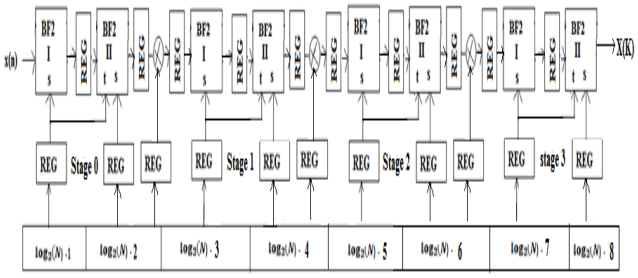

Fig.3. Block diagram for $Radix\ 2^2$ pipeline FFT processor for N=256

A $\log_2(N)$ bit binary counter serves two purposes: address counter for twiddle factor reading in each stages and synchronization controller.

The twiddle factors are applied at the butterfly output Z1 (n), and Z1 (n + N/2) is sent back to the shift registers to be "multiplied" in still next N/2 cycles when the first half of the next frame of time sequence is loaded. The operation of the second butterfly is same as that of the first one and the trivial twiddle factor multiplication has been implemented by real-imaginary swapping with a commutator and controlled add/subtract operations, as in Fig.1&2.

IV. IMPLEMENTATION OF THE PROPOSED FFT IN OFDM COMMUNICATION SYSTEM

The fundamental principle of the OFDM system is to decompose the high rate data stream (bandwidth=*W*) into *N* lower rate data streams and then to transmit them simultaneously over a large number of subcarriers. The IFFT is used for modulation and the FFT are used for demodulation. The data constellations on the orthogonal subcarriers in OFDM system is done by QPSK modulation for easy of designing. The transmitter and receiver blocks contain the FFT and IFFT modules. The FFT processor must finish the transform within the time to serve the purpose in the OFDM system. This FFT architecture effectively fits into the system

V. QUADRATURE PHASE SHIFT KEYED (QPSK) MODULATION

An OFDM carrier signal is the sum of a number of orthogonal sub-carriers, with message data on each subcarrier being independently modulated commonly using some type of quadrature phaseshift keying (QPSK).This composite message signal is typically used to modulate a main RF carrier. *s*[*n*] is a serial stream of input binary digits. At transmitter these are first demultiplexed into *N* parallel streams by inverse multiplexing, and each one mapped to a

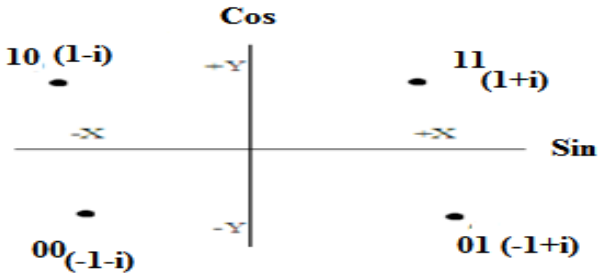

Fig.4 Constellation diagram of a QPSK modulated carrier

(possibly complex) symbol stream using some modulation constellation (QPSK). Note that the constellations may be different, so some streams may carry a higher bit-rate than others.

QPSK modulated carrier undergoes four distinct changes in phase that are represented as symbols and can take on the values of π/4, 3π/4, 5π/4, and 7π/4. Each symbol represents two binary bits of data this binary data is mapped into complex data.. The QPSK modulated carrier constellation diagram is shown in Fig.4.

VI. IMPLEMENTATION IN VERILOG

VERILOG Hardware Description Language (VERILOG) was introduced by Gateway Design Automation in 1984 as a proprietary hardware description and simulation language. Logic-circuit structures created by VERILOG synthesis tools directly from VERILOG behavioral descriptions, and target them into a preferred technology for realization.

By using VERILOG, It is easy to design, simulate, and synthesize anything form a simple combinational circuit to a complete microprocessor based system on a chip. It started out as documentation and modeling language, allows the behavior of digital-system designs to be precisely specified, simulated and language specification allows multiple modules to be stored in a single text file. All these features of VERILOG will help better in simulation and synthesis of proposed architecture. The OFDM Transmitter and Receiver presented above has been fully coded in VERILOG Hardware Description Language (VERILOG). Once the design is coded in VERILOG, the simulations and synthesis report is carried out by using Modelsim XEIII 6.2c compiler and the Xilinx Foundation ISA Environment 9.2i.

VII. RESULTS

The radix-4 Single-Path Delay-Commutator (R4SDC) and radix-2^2 pipeline architectures provide the highest Computational efficiency and were selected for implementation. The R4SDC architecture is interesting due to the computational efficiency of its addition; however the controller design is complex. The R2^2 pipeline architecture reduces the delays in all stages and increases the data rates.

The RTL schematic diagram for QPSK modulator is shown in fig.5.

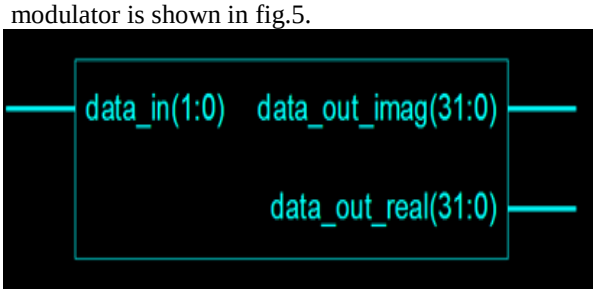

Fig.5 RTL schematic diagram for QPSK modulator

The device utilization summary for QPSK modulator is listed in table.1.

Table:1 Device utilization summary for QPSK modulator

Logic utilization	Used	Available	Utilization
Number of Slices	49	2448	2%
Number of IOs	66		
Number of bonded IOBs	66	172	38%

The RTL schematic diagram for FFT is shown in fig.6.

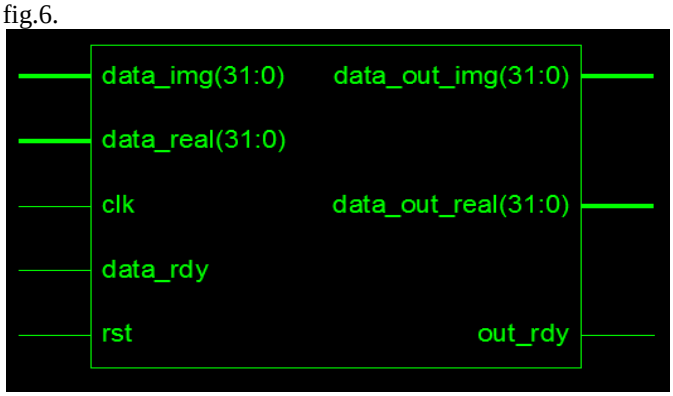

Fig.7 RTL schematic diagram for FFT

Table:2 Device utilization for FFT

Logic utilization	Used	Available	Utilization
Number of Slices	2978	3275	90%
Number of Slice Flip Flops	1678	7532	22%
Number of 4 input LUTs	5236	6874	76%
Number of IOs	132		
Number of bonded IOBs	132	172	76%
Number of MULT18X18SIOs	9	12	75%
Number of GCLKs	1	24	4%

The figure.8 shows the simulated wave form of the OFDM communication system. When mess_ready is 'Low' there is no data transmission. When it is 'High', then the input data constellation is done and applied to the IFFT at the transmitter. When Rx_data is 'High' then the data is received by FFT at the receiver. Pcnt (packet count) indicates that the no. of packets is sent to the receiver.

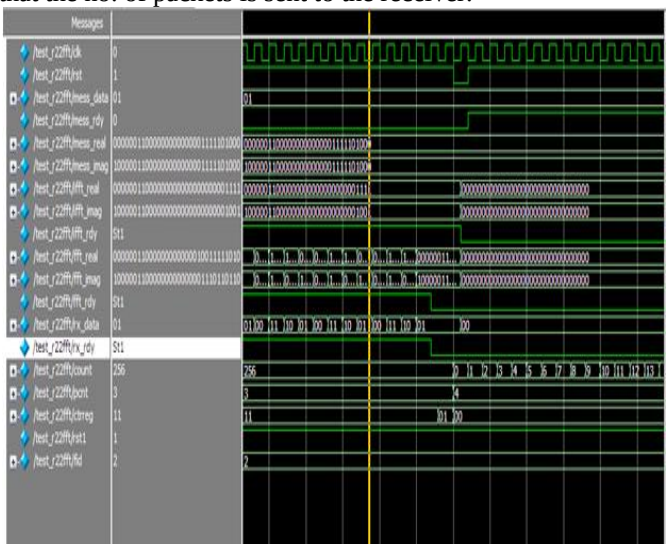

Fig.8. Simulated waveform showing that data transmission in OFDM System

VIII. CONCLUSIONS AND FUTURE WORK

This paper describes the design of modified Radix2^2 pipelined FFT processor with N=256 points to provide the higher data rates in OFDM. The proposed architecture has three main advantages (1) Fewer butterfly iteration to reduce power consumption, (2) Pipeline of Radix2^2 butterfly to speed up clock frequency, (3) Even distribution of memory access to make utilization efficiency of components.

In summary, the speed performance of this design easily satisfies most application requirements of mobile WiMAX 802.16e, 802.11-based wireless LANs those uses OFDM modulated wireless communication system. The implemented design gives an easy way to increase the number of points of FFT as well as IFFT by imposing simple modification. Future work can includes the development of complete OFDM system and upgrade it to a multiple input multiple outputs (MIMO) system.

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